DANIEL **KELLER**

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WORK EXPERIENCE

JUNE 2024 - PRESENT

PHD STUDENT / DIGITAL IC DESIGN ENGINEER, CSEM SA

- Working on the SoC business unit, working on ULP ASICs on a mixed analog and digital team.
- Researching on ML accelerators in the edge.
- Active contributing to PULP open-source platform.
- Implementation of DMA on SoC for high efficient data movement for TCDM memory on PULP clusters.

DECEMBER 2023 - MAY 2024

DIGITAL IC DESIGN ENGINEER, INCIRT GMBH

- Implementing DSP functionality on hardware using SystemVerilog/Verilog and using HLS (High Level Synthesis) to implement the C++ algorithms.
- Testbench implementation.
- Responsible for the full RTL-to-GDSII flow from Synthesis to PNR and Signoff (delivering an LVS and DRC clean „block")
- Programming/scripting languages (Python, C++, TCL)

NOVEMBER 2022 – DECEMBER 2023

ANALOG/MIXED-SIGNAL DESIGN ENGINEER, INCIRT GMBH

- Digital Design - leading 3 consecutive successful tape-outs (Global Foundries 22nm FDSOI)
- System Modelling of RF SoC
- RTL to GDSII full flow implementation to timing closure

JANUARY 2022 – OCTOBER 2022

STUDENT ASSISTANT, CHAIR OF HIGH FREQUENCY ELECTRONICS – RWTH AACHEN UNIVERSITY

- DSP Digital Design ASIC
- FPGA design

JULY 2020 – DECEMBER 2021

IT INFRASTRUCTURE ENGINEER, METLIFE

- Led annual country mainframe PaaS disaster recovery to DR data centre in Poland.
- Supported enterprise systems management, IAM and PAM enforcing policies.

NOVEMBER 2019 – MAY 2020

INFORMATION TECHNOLOGY TRAINEE, METLIFE

- Proactively recognised potential trends based on call volume and incident review while providing resolutions, new/enhanced trainings, tools, and process leading to improved user support.

EDUCATION

JUNE 2024 – PRESENT (JUNE 2028)

DOCTOR OF SCIENCE, ELECTRICAL AND COMMUNICATIONS ENGINEERING, ETH ZÜRICH

Supervised by Prof. Luca Benini and collaborating on the open-source platform PULP.

- Topic on ML accelerators and ULP SoC design.

NOVEMBER 2020 – FEBRUARY 2024

M. SC. ELECTRICAL ENGINEERING, INFORMATION TECHNOLOGY AND COMPUTER ENGINEERING, RWTH AACHEN UNIVERSITY

Master of science in Communications Engineering.

- Master thesis: "Analysis and design of the digital signal processor for a wide bandwidth FD-ADC based receiver"

NOVEMBER 2020 – APRIL 2021

CISCO NETWORKING ACADEMY, CISCO NETWORKING ACADEMY

Cisco Engineer Incubator, Incubator Program 8.0.

SEPTEMBER 2013 – NOVEMBER 2020

DEGREE IN TELECOMMUNICATION ENGINEERING, TELECOMMUNICATION SYSTEMS, UNIVERSIDAD POLITÉCNICA DE MADRID

Engineering degree.

- Bachelor thesis on Mask R-CNN in warehouses (Machine Learning).

TECHNICAL EXPERTISE

- Systemverilog, Verilog
- SystemC, C++ (Cadence Stratus HLS)
- Cadence Digital tools RTL to GDSII (Genus, Innovus, Tempus, Quantus)
- Python, Java, TCL, C
- MATLAB and Simulink
- Cadence Virtuoso (for advance nodes)
- FPGA design (Xilinx Vivado)
- PCB design Altium and Cadence Allegro
- CST Microwave Studio

LANGUAGES

- **Spanish** – Native or bilingual proficiency
- **English** – Native or bilingual proficiency
- **German** – Full professional proficiency

TECHNICAL CERTIFICATES

- **Cadence:** Cadence RTL-to-GDSII Flow, Basic Static Timing Analysis, Innovus Hierarchical Implementation
- **MathWorks**: MATLAB Onramp, MATLAB fundamentals.
- **DeepLearning.ai/Coursera**: Neural Networks and Deep Learning and Convolutional Neural Networks.
- **Stanford University/Coursera**: Machine Learning.